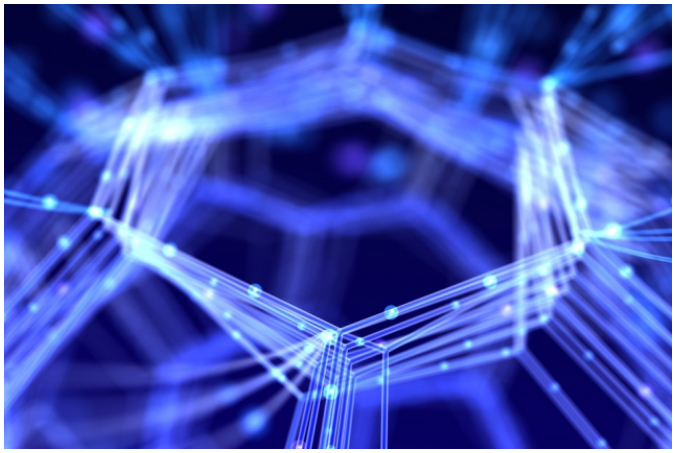
Scientists at Stanford and MIT take on the communications bottleneck separating the storage and processing of data-- bringing about a 3D chip combining processing and storage through breakthrough nanotechnologies.



As the researchers put it, current computers waste a lot of time and energy shuffling data between storage and processing. The amount of data produced by the modern world is increasing at a rapid rate, while we are reaching the physical limit as to by how much silicon transistors can be improved.

Enter the Stanford-MIT 3D chip. It is built using carbon nanotubes, sheets of 2D graphite formed into nanocylinders, and resistive random-access memory (RRAM), a type of memory built using a "solid dielectric material." The actual prototype stacks 1 million RRAM cells on 2 million carbon nanotube transistors, making a "dense 3D computer architecture with interleaving layers of logic and memory." Bringing the layers together are ultradense wires, resolving the communication bottleneck.

“The devices are better: Logic made from carbon nanotubes can be an order of magnitude more energy-efficient compared to today’s logic made from silicon, and similarly, RRAM can be denser, faster, and more energy-efficient compared to DRAM,” the researchers say.

The 3D chip promises to be more energy efficient on the production side, since carbon nanotube circuits and RRAM memory can be fabricated at temperatures below 200 degrees Centigrade (in comparison silicon transistors require temperatures of over 1000 C). In addition, the technology is shown to be compatible with current silicon infrastructure, both in terms of fabrication and design.

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