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A collaboration between IBM, Samsung and Global Foundries brings about an industry firsts--silicon nanosheet transistors allowing the production of 5 nanometer (nm) chips.

Presented at the 2017 Symposia on VLSI Technology and Circuits conference in Kyoto, Japan, the process arrives just 2 years after the development of a 7nm test node chip with 20 billion transistors, paving the way for 30 billion switches on a "fingernail-sized" chip.

As Big Blue puts it, the breakthrough uses "stacks of silicon nanosheets" to build the transistor instead of FinFET architecture, the current blueprint for the semiconductor industry. It promises a 40% performance enhancement at fixed power, or 75% power savings at matched performance, bringing about a "significant" boost in the performance of anything from AI systems to VR and mobile devices.

Building the silicon nanosheets involved the Extreme Ultraviolet (EUV) lithography employed in the production of the 7nm test node. EUV lithography allows the continuous adjustment of nanosheet width within a single manufacturing process or chip design. This permits the fine-tuning of performance and power in specific circuits, something not possible with FinFET production.

“For business and society to meet the demands of cognitive and cloud computing in the coming years, advancement in semiconductor technology is essential,” IBM adds. “That’s why IBM aggressively pursues new and different architectures and materials that push the limits of this industry, and brings them to market in technologies like mainframes and our cognitive systems.”

Of course, seeing how 7nm chips are still to hit the market, we will have to wait a while until 5nm reaches the industry at large.

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