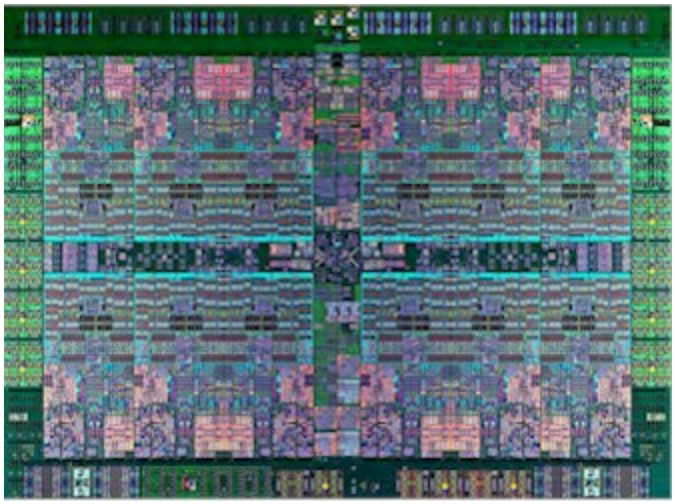
IBM shows off the latest generation of Power processors at the 2013 Hot Chips conference with the Power8 chip, a 12-core processor designed for cloud-based data centre applications.



Seen in prototype form, the Power8 measures 650 square millimetres (making it slightly bigger than the Power7+) and is built using the 22nm process with coper and silicon-on-insulator technologies.

Data transfer rates within the chip clock at 230GB per second, with 512KB of cache per core, 96MB on-chip cache and 128MB off-chip L4 cache.

The 12 cores feature a total of 16 execution cores, with 2 load store units (LSUs), ondition register unit (CRU), branch register unit (BRU) and 2 instruction fetch units (IFUs). It also has 2 fixed-point units (FXUs), 2 vector math units (VMXs), decimal floating unit (DFU) and a cryptographic unit.

Each core has 8 threads implemented via simultaneous multithreading (SMT). SMT is dynamically tuneable, allowing each core to have 1, 2, 4 or 8 threads fired up.

One can connect external components via CAPI (Coherence Attach Processor Interface) port, which in turn interfaces with the PCIe slot for external components such as GPUs or FFGAs.

The Power8 chip is the foundation of the OpenPOWER Consortium-- the Big Blue effort to boost the popularity of Power architecture by licensing IBM server hardware and firmware. The Consortium currently counts Google, Mellanox, Nvidia and Tyan as members, and will allow datacentre customers to develop own Power-based hardware.

IBM gives no say when the Power8 chip will see release.

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