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23 March 2018

Semiconductor specialist Xilinx presents what it claims is a chip with capabilities superseding the field-programmable gate array (FPGA)-- the adaptive compute acceleration platform (APAC).

FPGAs are integrated circuits one can further configured after manufacturing. They find use as accelerators in large-scale high performance computing (HPC) and supercomputing environments, as well as cloud computing datacentres and Internet of Things (IoT) hardware. Xilinx says the ACAP goes a step beyond FPGAs. A "highly integrated multi-core heterogeneous compute platform," the ACAP can not only be changed at the hardware level to adapt to a range of applications and workloads, but adapts dynamically during operations for "levels of performance and performance per-watt that is unmatched by CPUs or GPUs."

The company claims ACAPs can be used in applications as varied as video transcoding, database, data compression, search, AI inference, genomics, machine vision, computational storage and network acceleration. The actual chip consists of memory and hardware-programmable DSP blocks, a multicore SoC and one or more software programmable (and hardware adaptable) compute engines, all connected via network on chip (NoC). Also included is integrated programmable I/O functionality, ranging from integrated hardware programmable memory controllers, advanced SerDes technology and leading edge RF-ADC/DACs, t integrated High Bandwidth Memory (HBM) depending on the device variant.

In turn software developers can target APAC-based systems with tools such as C/C++, OpenCL and Python, as well as program ACAPs at the RTL level using FPGA tools. Either way, Xilinx promises a 20x performance boost on deep neural networks compared to the latest 16nm Virtex VUP9 FPGA, and Everest-based 5G remote radio heads with 4x the bandwidth versus the latest 16nm radios.

The first APAC product to hit the market is "Everest," a chip based on the TSNM 7nm process slated for release later this year.

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