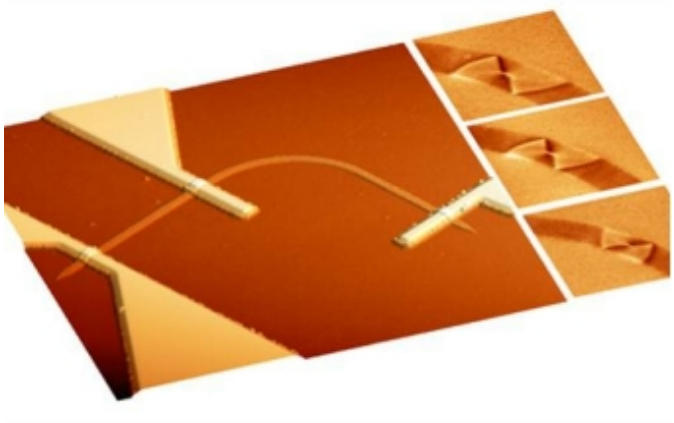
IBM calls it "Racetrack Memory" even if it has nothing to do with neither cars nor horses-- but it might lead to future memory chips with the capacities of HDDs and the performance and durability of SSDs.



The company recently announced it has a working Racetrack Memory circuit at the IEEE International Electron Devices conference, with a chip consisting of 256 Racetrack "cells." Each cell consists of a nanowire 240nm wide and 20nm thick, with "spin currents" (electric currents, in other words) manipulating the magnetic state of the nano-scale magnetic regions within the nanowires.

IBM claims the test chip reaches DRAM-level I/O speeds, with greater durability than even current NAND flash technology, leading to "a new type of data-centric computing that allows massive amounts of stored information to be accessed in less than a billionth of a second." Exciting.

Other kinds of future memory technologies researchers at IBM (and elsewhere) are working on include graphene (a derivative of graphite, the stuff inside the humble pencil) and the fantastically named "carbon nanotubes." The name which might suggest something out of Buck Rogers, but it actually refers to transistors of sub-10nm channel lengths IBM says beat silicon-based devices of the same sizes.

The development of new non-volatile memory is vital-- the smaller the technology gets, the further NAND flash development is (potentially) limited. As silicon memory cell walls become increasingly thinner, electrons start leaking out to other cells, causing data errors and demanding more sophisticated error correction code.

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